

TITLE OF THE INVENTION

5 POWER MOS TRANSISTOR HAVING TRENCH GATE

CROSS-REFERENCE TO RELATED APPLICATIONS

*PC  
8/15/07*  
*is a continuation of U.S. patent application 09/667,559 FILED 09/22/2000, abandoned, which*  
This application claims benefit of priority under 35 U.S.C. 119 to Japanese Patent

Application No. P11-269922 filed September 24, 1999, the entire contents of which are

10 incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a structure of a power MOS transistor having a  
15 trench gate.

Discussion of the Background

Fig. 1 is a plan view showing a spline-structured MOS transistor manufactured  
based on current product design rules. Trench gates 45 and source contacts 46 are  
alternately formed on a semiconductor substrate. Each of the source contacts 46 is connected  
20 to a source electrode formed on a layer formed further thereon.

Fig. 2 is an upper surface view showing a pattern of an offset mesh-structured  
MOS transistor manufactured based on current product design rules. Trench gates 38 and  
source contacts 44 are alternately formed on a semiconductor substrate. Each of the  
source contacts 44 is connected to a source electrode formed on a layer formed further  
25 thereon. The offset mesh type is designed to realize a high degree of integration by